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10/085,581	02/26/2002	Yu-Cheun Jou	020278	8984

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Qualcomm Incorporated
Patents Department
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EXAMINER	
PATEL, NIRAV B	

ART UNIT	PAPER NUMBER
2135	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/085,581	JOU ET AL.	
	Examiner	Art Unit	
	Nirav Patel	2135	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☒ Claim(s) *5,10,24 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1 -(5/28/02)*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the application filed on 2/26/02.

2. Claims 1-38 are under examination.

Claim Objections

Claims 5, 10, 24 and 29 are objected to because of the following informalities:

"*performing and exclusive-OR*" should be "*performing an exclusive-OR*" at claims 5, 10, 24 and 29, line 3.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 5, 6, 10-12, 16, 20, 24, 25, 29, 30, 31 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ragavan et al (US Patent No. 4,811,394) and in view of Chan et al (US Pub No. 2002/0089935).

As per claim 1, Ragavan teaches:

determining a scrambling sequence in accordance with a metric of system time (i.e. clock signal) **[*col. 4 lines 27-34* "In the scrambler circuit of FIG. 1, a storage register 10, which may for example comprise a 22-bit storage register, stores the initial scrambling sequence value which is then loaded into a 22-bit PN sequence generator 12 in response to a start pulse. Having been loaded with this value, the sequence generator then proceeds to generate its PN sequence in response to a clock signal" Fig. 1]**; and scrambling information bits (i.e. clear text) with the scrambling sequence **[Fig. 1].**

Ragavan doesn't clearly teach that metric of system time. However, Chan teaches that metric of system time **[*paragraph 0047, lines 1-5* "a channel condition estimation metric may be calculated using one or more metrics including frame error rate (FER) metric, signal to noise ratio estimate (SNR) metric, energy per bit (Eb)/Thermal noise (Nt) estimate metric, and system time and/or finger time drift rate"].**

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teaching of Chan into the teaching of Ragavan to calculate metric using system time. The modification would be obvious because one of ordinary skill in the art would be motivated to generate metric for indicating the channel condition, which determines the optimal packet-size. An optimal RLP packet-size that equipped with CRC bits, so it prevents the RLP packet from getting rejected due to bit errors **[Chan, *paragraph 0007, lines 2-12*].**

As per claim 5, the rejection of claim 1 is incorporated and further Ragavan teaches that performing an exclusive-OR of the information bits (i.e. clear text) with the scrambling sequence **[Fig. 1 *col. 4 lines 34-35* "with the PN sequence being combined with clear text data in an Exclusive OR (EOR) gate"].**

As per claim 6, Ragavan teaches:

determining an unscrambling sequence in accordance with a metric of system time (i.e. clock signal) **[*col. 4 lines 36-39* " in the descrambler circuit of fig. 2, a similar 22-bit storage register 20 stores a initial scrambling sequence value which is loaded into an identical 22-bit PN sequence generator 22 in response to a start pulse, Fig. 2]**; and

unscrambling information bits with the unscrambling sequence **[Fig. 2].**

Ragavan doesn't clearly teach that metric of system time. However, Chan teaches that metric of system time **[*paragraph 0047, lines 1-5* "a channel condition estimation metric may be calculated using one or more metrics including frame error rate (FER) metric, signal to noise ratio estimate (SNR) metric, energy per bit (Eb)/Thermal noise (Nt) estimate metric, and system time and/or finger time drift rate"].**

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teaching of Chan into the teaching of Ragavan to calculate metric using system time. The modification would be obvious because one of ordinary skill in the art would be motivated to generate metric

for indicating the channel condition, which determines the optimal packet-size. An optimal RLP packet-size that equipped with CRC bits, so it prevents the RLP packet from getting rejected due to bit errors **[Chan, *paragraph 0007, lines 2-12*].**

As per claim 10, the rejection of claim 6 is incorporated and is rejected for the same reason set forth in the rejection of claim 5 above.

As per claim 11, is rejected for the same reason set forth in the rejection of claims 1 and 6 above.

As per claim 12, Ragavan teaches:

determining the scrambling sequence in accordance with the metric of system time (i.e. clock signal) **[*col. 4 lines 27-34* "In the scrambler circuit of FIG. 1, a storage register 10, which may for example comprise a 22-bit storage register, stores the initial scrambling sequence value which is then loaded into a 22-bit PN sequence generator 12 in response to a start pulse. Having been loaded with this value, the sequence generator then proceeds to generate its PN sequence in response to a clock signal" Fig. 1]**; and scrambling information bits (i.e. clear text) with the scrambling sequence **[Fig. 1].**

Ragavan doesn't clearly teach that metric of system time. However, Chan teaches that metric of system time **[*paragraph 0047, lines 1-5* "a channel condition estimation metric may be calculated using one or more metrics including frame**

error rate (FER) metric, signal to noise ratio estimate (SNR) metric, energy per bit (Eb)/Thermal noise (Nt) estimate metric, and system time and/or finger time drift rate"].

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teaching of Chan into the teaching of Ragavan to calculate metric using system time. The modification would be obvious because one of ordinary skill in the art would be motivated to generate metric for indicating the channel condition, which determines the optimal packet-size. An optimal RLP packet-size that equipped with CRC bits, so it prevents the RLP packet from getting rejected due to bit errors **[Chan, *paragraph 0007, lines 2-12*].**

As per claim 16, Ragavan teaches:

determining an unscrambling sequence in accordance with a metric of system time (i.e. clock signal) **[*col. 4 lines 36-39* " in the descrambler circuit of fig. 2, a similar 22-bit storage register 20 stores a initial scrambling sequence value which is loaded into an identical 22-bit PN sequence generator 22 in response to a start pulse, Fig. 2]**; and

unscrambling information bits with the unscrambling sequence **[Fig. 2].**

Ragavan doesn't clearly teach that metric of system time. However, Chan teaches that metric of system time **[*paragraph 0047, lines 1-5* "a channel condition estimation metric may be calculated using one or more metrics including frame error rate (FER) metric, signal to noise ratio estimate (SNR) metric, energy per bit**

(Eb)/Thermal noise (Nt) estimate metric, and system time and/or finger time drift rate"].

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teaching of Chan into the teaching of Ragavan to calculate metric using system time. The modification would be obvious because one of ordinary skill in the art would be motivated to generate metric for indicating the channel condition, which determines the optimal packet-size. An optimal RLP packet-size that equipped with CRC bits, so it prevents the RLP packet from getting rejected due to bit errors **[Chan, *paragraph 0007, lines 2-12*].**

As per claim 20, it is an apparatus claim corresponds to a method claim 1 and is rejected for the same reason set forth in the rejection of claim 1 above.

As per claim 24, the rejection of claim 20 is incorporated and further claim 24 is an apparatus claim corresponds to method claim 5 and is rejected for the same reason set forth in the rejection of claim 5 above.

As per claim 25, it is an apparatus claim corresponds to a method claim 6 and is rejected for the same reason set forth in the rejection of claim 6 above.

As per claim 29, the rejection of claim 26 is incorporated and further claim 26 is an apparatus claim corresponds to method claim 5 and is rejected for the same reason set forth in the rejection of claim 5 above.

As per claim 30, it is an apparatus claim corresponds to method claims 1 and 6. Claim 30 is rejected for the same reason set forth in the rejection of claims 1 and 6 above.

As per claim 31, it is an apparatus claim corresponds to method claim 12 and is rejected for the same reason set forth in the rejection of claim 12 above.

As per claim 35, it is an apparatus claim corresponds to method claim 16 and is rejected for the same reason set forth in the rejection of claim 16 above.

4. Claims 2, 3, 7, 13-14, 17, 21, 22, 26, 32, 33 and 36 are rejected under 35 USC 103 (a) for being unpatentable over Ragavan et al (US Patent No. 4,811,394) in view of Chan et al (US Pub No. 2002/0089935) and further in view of Johnson et al (US Patent No. 6,487,181).

As per claim 2, the rejection of claim 1 is incorporated. Chan teaches that determine the metric in accordance with a system time **[*paragraph 0047 lines 1-5*]**. Ragavan and Chan don't teach that determining the metric in accordance with a

subinterval of a system time interval (i.e. time slot or slot) in which the information bits are to be transmitted.

However, Johnson teaches that determine the metric in accordance with a *subinterval of a system time interval (i.e. time slot or slot)* **[*col. 2 lines 50-52* "the communication device determines an error metric for the encoded time slot" abstract line 1-2 a communication device employs a method and apparatus for transmitting and receiving information in a time slot"].**

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teaching of Johnson into the teaching of Ragavan and Chan to determine the metric for the time slot. The modification would be obvious because one of ordinary skill in the art would be motivated to determine the metric for time slot (which contains the information) and determine the truncated time slot. The truncated time slot consume less power than the transmission of a completely filled time slot, and result in an increased rechargeable life of the power source **[Johnson, *col. 9 lines 23-28*].**

As per claim 3, the rejection of claim 2 is incorporated and further Johnson teaches that first subinterval of the system time interval (i.e. time slot or slot) **[*col. 2 lines 42-44* "first portion of the time slot"].**

As per claim 7, the rejection of claim 6 is incorporated and Chan teaches that determine the metric in accordance with a system time **[paragraph 0047 lines 1-5].**

Ragavan and Chan don't teach that determine the metric in accordance with a first *subinterval of a system time interval (i.e. time slot or slot)* and second subinterval comprises information bits.

However, Johnson teaches that determine the metric in accordance with a first *subinterval of a system time interval (i.e. time slot or slot)* **[*col. 2 lines 50-52* "the communication device determines an error metric for the encoded time slot" *col. 2 lines 42-44* "first portion of the time slot"]** and second subinterval comprises information bits **[*col. 3 lines 65-67, col. 4 lines 1-2* "insert user information symbols 212,213 into a first portion of the four frequency sub-channels 201-204 in time slot 200 and inserts channel-related information symbols 210, 211 into a second portion of the time slot 200"].**

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teaching of Johnson into the teaching of Ragavan and Chan to determine the metric for the time slot. The modification would be obvious because one of ordinary skill in the art would be motivated to determine the metric for time slot (which contains the information) and determine the truncated time slot. The truncated time slot consume less power than the transmission of a completely filled time slot, and result in an increased rechargeable life of the power source **[Johnson, *col. 9 lines 23-28*].**

As per claim 13, the rejection of claim 12 is incorporated and is rejected for the same reason set forth in the rejection of claim 2 above.

As per claim 14, the rejection of claim 13 is incorporated and is rejected for the same reason set forth in the rejection of claim 3 above.

As per claim 17, the rejection of claim 16 is incorporated and is rejected for the same reason set forth in the rejection of claim 7 above.

As per claim 21, the rejection of claim 20 is incorporated and further claim 21 is an apparatus claim corresponds to method claim 2 and is rejected for the same reason set forth in the rejection of claim 2 above.

As per claim 22, the rejection of claim 21 is incorporated and further claim 22 is an apparatus claim corresponds to method claim 3 and is rejected for the same reason set forth in the rejection of claim 3 above.

As per claim 26, the rejection of claim 25 is incorporated and further claim 26 is an apparatus claim corresponds to method claim 7 and is rejected for the same reason set forth in the rejection of claim 7 above.

As per claim 32, the rejection of claim 31 is incorporated and further claim 32 is an apparatus claim corresponds to method claim 2 and is rejected for the same reason set forth in the rejection of claim 2 above.

As per claim 33, the rejection of claim 32 is incorporated and further claim 33 is an apparatus claim corresponds to method claim 3 and is rejected for the same reason set forth in the rejection of claim 3 above.

As per claim 36, the rejection of claim 35 is incorporated and further claim 36 is an apparatus claim corresponds to method claim 7 and is rejected for the same reason set forth in the rejection of claim 7 above.

5. Claims 4, 9, 23, and 28 are rejected under 35 USC 103 (a) for being unpatentable over Ragavan et al (US Patent No. 4,811,394) in view of Chan et al (US Pub No. 2002/0089935) in view of Johnson et al (US Patent No. 6,487,181) and further in view of Wei et al (US Patent No. 6,348,876).

As per claim 4, the rejection of claim 2 is incorporated. Ragavan, Chan and Johnson don't teach that mapping of the metric on the scrambling sequence.

However, Wei teaches the mapper (i.e. to map the metric on the scrambling sequence) **[Fig. 7 *col. 6 lines 59-61* "the scrambled data is then, in block 704, divided into symbols that are mapped to signal point in the QAM constellation"].**

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teaching of Wei into the

teaching of Ragavan, Chan and Johnson to utilize the mapper for mapping the metric on the scrambling sequence. The modification would be obvious because one of ordinary skill in the art would be motivated to map the data or symbols to signal point or information using the mapper **[Wei, *col. 6 lines 59-60*]**.

As per claim 9, the rejection of claim 7 is incorporated and is rejected for the same reason set forth in the rejection of claim 4 above.

As per claim 23, the rejection of claim 21 is incorporated and further claim 23 is an apparatus claim corresponds to method claim 4 and is rejected for the same reason set forth in the rejection of claim 4 above.

As per claim 28, the rejection of claim 26 is incorporated and further claim 28 is an apparatus claim corresponds to method claim 4 and is rejected for the same reason set forth in the rejection of claim 4 above.

6. Claims 8, 18, 27 and 37 are rejected under 35 USC 103 (a) for being unpatentable over Ragavan et al (US Patent No. 4,811,394) in view of Chan et al (US Pub No. 2002/0089935) in view of Johnson et al (US Patent No. 6,487,181) and further in view of O'Connor (US Patent No. 4,677,617).

As per claim 8, the rejection of claim 7 is incorporated. Johnson teaches that determine the first subinterval of the system time interval (i.e. time slot) **[Fig. 6, col. 50-56]**. Ragavan, Chan and Johnson don't teach that the first subinterval *preceding* the second subinterval *by one subinterval.*

However, O'Connor teaches that first subinterval *preceding* the second subinterval *by one subinterval* **[Fig. 2, k-1 interval, k interval and k+1 interval (i.e. subinterval preceding by one subinterval)]**.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teaching of O'Connor into the teaching of Ragavan, Chan and Johnson to determine the number of time intervals of the present interval of system time or network time. The modification would be obvious because one of ordinary skill in the art would be motivated to achieve time synchronization between frequency hopping network communication units **[O'Connor, *col. 4 lines 30-39*]**.

As per claim 18, the rejection of claim 17 is incorporated and is rejected for the same reason set forth in the rejection of claim 8 above.

As per claim 27, the rejection of claim 26 is incorporated and further claim 27 is an apparatus claim corresponds to method claim 8 and is rejected for the same reason set forth in the rejection of claim 8 above.

As per claim 37, the rejection of claim 36 is incorporated and further claim 37 is an apparatus claim corresponds to method claim 8 and is rejected for the same reason set forth in the rejection of claim 8 above.

7. Claims 15, 19, 34 and 38 are rejected under 35 USC 103 (a) for being unpatentable over Ragavan et al (US Patent No. 4,811,394) in view of Chan et al (US Pub No. 2002/0089935) and further in view of Wei et al (US Patent No. 6,348,876).

As per claim 15, the rejection of claim 12 is incorporated. Ragavan and Chan don't teach that mapping of the metric on the scrambling sequence.

However, Wei teaches the mapper (i.e. to map the metric on the scrambling sequence) **[Fig. 7 *col. 6 lines 59-61* "the scrambled data is then, in block 704, divided into symbols that are mapped to signal point in the QAM constellation"].**

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teaching of Wei into the teaching of Ragavan, Chan and Johnson to utilize the mapper for mapping the metric on the scrambling sequence. The modification would be obvious because one of ordinary skill in the art would be motivated to map the data or symbols to signal point or information using the mapper **[Wei, *col. 6 lines 59-60*]**.

As per claim 19, the rejection of claim 16 is incorporated and is rejected for the same reason set forth in the rejection of claim 15 above.

As per claim 34, the rejection of claim 31 is incorporated and is rejected for the same reason set forth in the rejection of claim 15 above.

As per claim 38, the rejection of claim 35 is incorporated and is rejected for the same reason set forth in the rejection of claim 15 above.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

You et al (US 2003/0103480) – Error detection code generation method and error detection code generator.

You et al (US 2003/0147422) – Method for Scrambling Packet data Using variable slot length and apparatus thereof.

Cheng (US 2003/0012372) – System and method for joint encryption and error-correcting coding.

Taipale (US 6,310,856) discloses that a wideband CDMA handset (20) has a receiver (50) which simplifies initial sequence acquisition. The receiver (50) includes an efficient searcher receiver (54) which searches for long code mask sequences (LMS) using two correlators (80, 100)

McDonough et al (US 6,748,006) discloses unique methods and apparatus for maintaining timing in spread spectrum communications.

Kim et al (US 6,438,119) discloses that a CDMA communication system provides a dedicated control channel capable of efficiently communicating control messages between a base station and a mobile station.

Cain (US 6,904,032) discloses a wireless communication network includes a plurality of mobile nodes each including a transceiver, a phased array antenna connected to the transceiver and a controller connected to the transceiver.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nirav Patel whose telephone number is 571-272-5936. The examiner can normally be reached on 8 am - 4:30 pm (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Vu can be reached on 571-272-3859. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NBP
8/5/05

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SUPERVISORY PATENT EXAMINER
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